

Learn Digital Design of Microcomputer Systems with Deeds

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RESEARCH OBJECTIVE

Designing a programmable D-PET flip-flop component waveform generator is the aim of this lab. As the time cycle of Figure 1 progresses, it creates six cyclic signals: D, PR, CL, CK, Q, and NOT Q.

DESIGN OF A PERIODIC SEQUENCE PROGRAMMABLE GENERATOR

The preset and clear input are active-low, because there are an inverting bubble at that input lead on the block symbol, just like the negative edge-trigger clock inputs. When the preset input is activated, the flip-flop will be reset ($Q=0$, $\bar{Q}=1$) regardless of any of the synchronous inputs or the clock. When the clear input is activated, the flip-flop will be set ($Q=1$, $\bar{Q}=0$), regardless of any of the synchronous inputs or the clock. So, what happens if both preset and clear inputs are not activated (both of them 0) ? Surprise, surprise: we get an invalid state on the output, where Q and \bar{Q} go to the same state. when both preset and clear inputs are activated then the flip flop will work normally

Diagram 2. The flip flop is a basic building block of sequential logic circuits.

It is a circuit that has two stable states and can store one bit of state information.

The output changes state by signals applied to one or more control inputs.

The basic D Flip Flop has a D (data) input and a clock input and outputs Q and \bar{Q} (the inverse of Q). Optionally it may also include the PR (Preset) and CLR (Clear) control inputs

Diagram 3.

INPUTS			OUTPUTS		
PR	CLR	CLK	D	Q	\bar{Q}
0	1	X	X	1	0
1	0	X	X	0	1
0	0	X	X	X	X
1	1	↑	1	1	0
1	1	↑	0	0	1
1	1	0	X	Q_0	\bar{Q}_0

Diagram 2

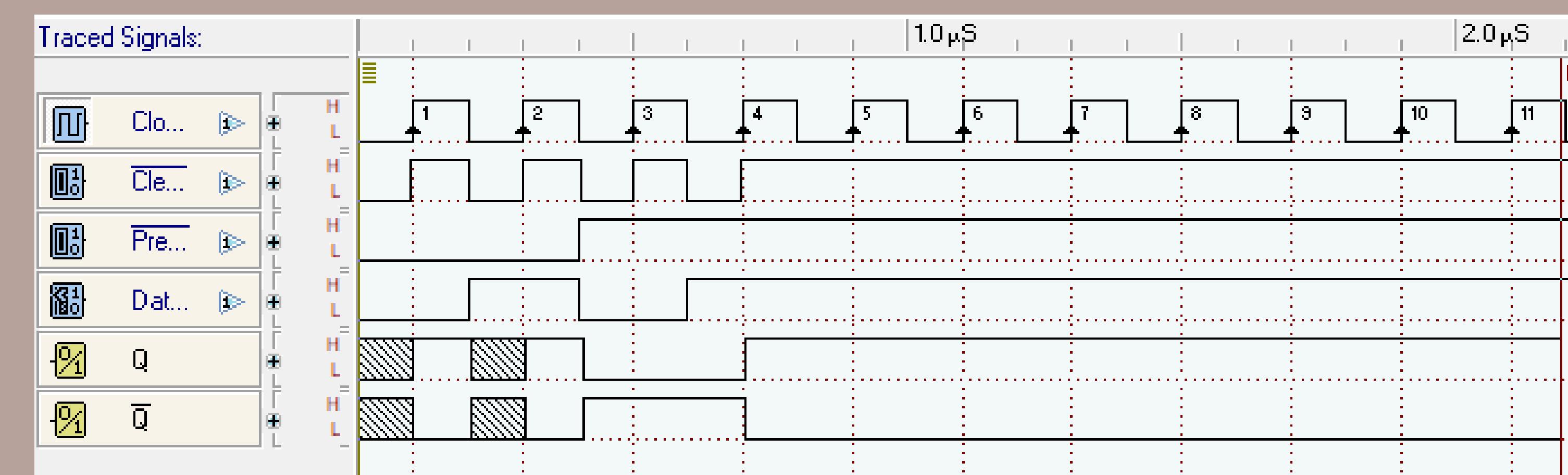


Diagram 1.

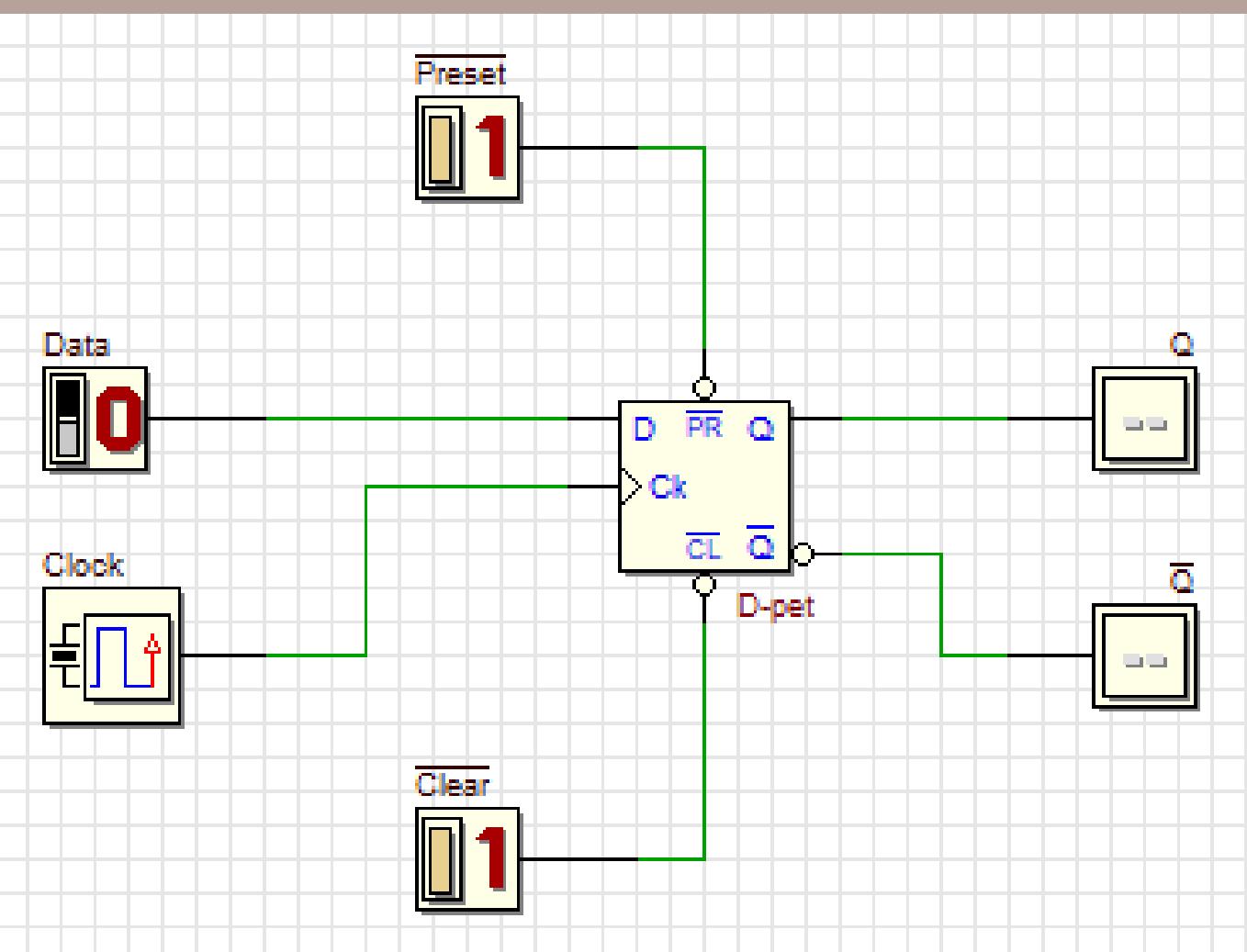
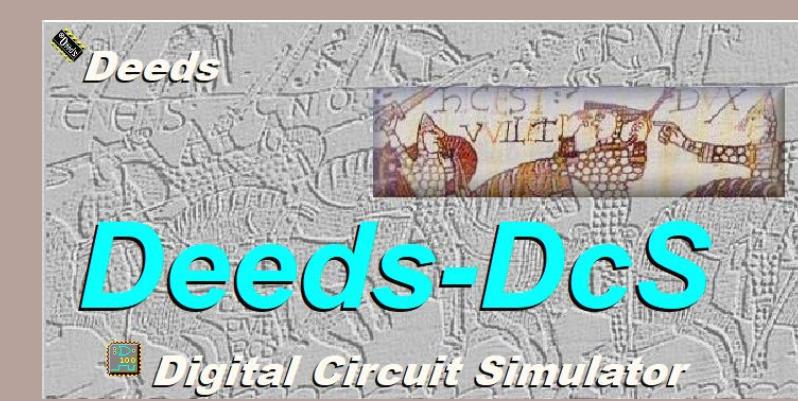


Diagram 3.



INTERNATIONAL COMMUNITY FORUM (ICF)



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- [2] https://www.digitalelectronicsdeeds.com/learningmaterials/LM/T030/030160_Timing_Analysis_D_PET_FF_comp/Index.htm
<instructables.com/D-Flip-Flop-With-Preset-and-Clear/>