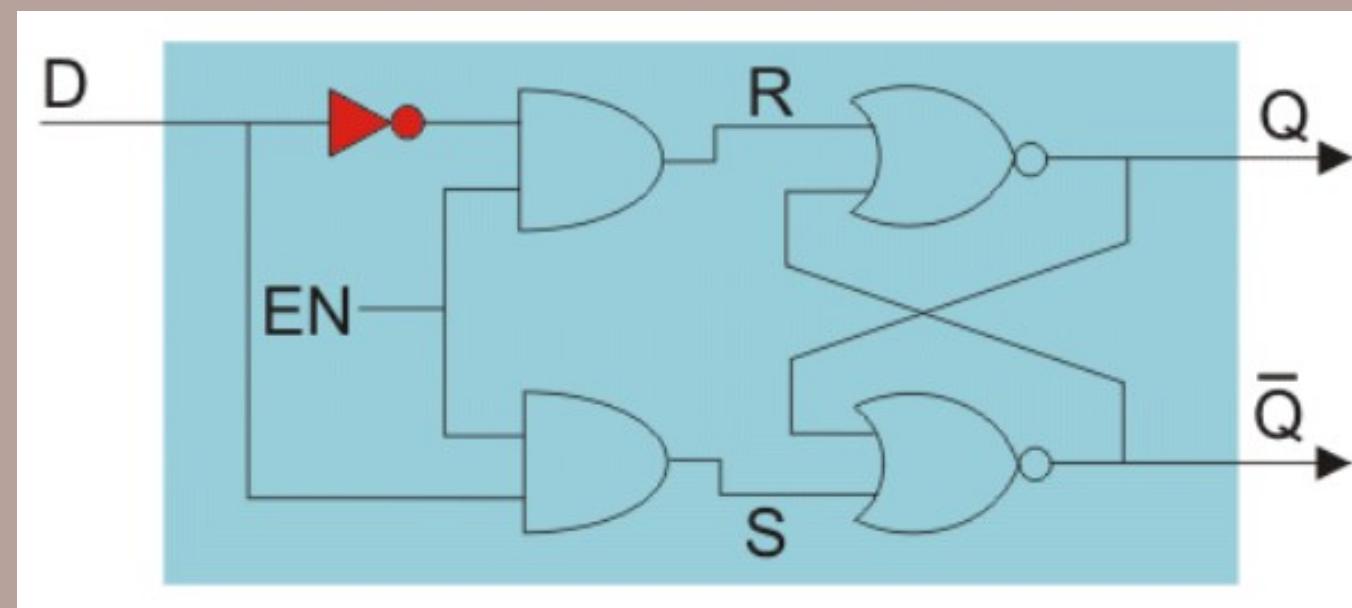
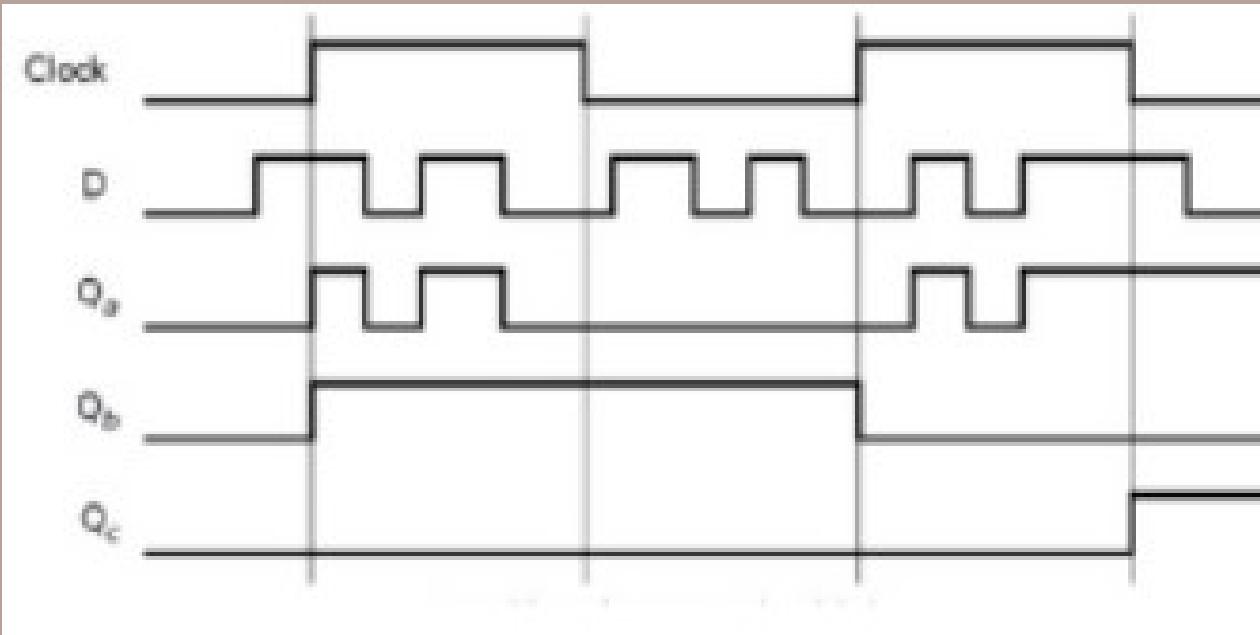


Learn the analysis of a D-Latch Flip-Flop with Deeds



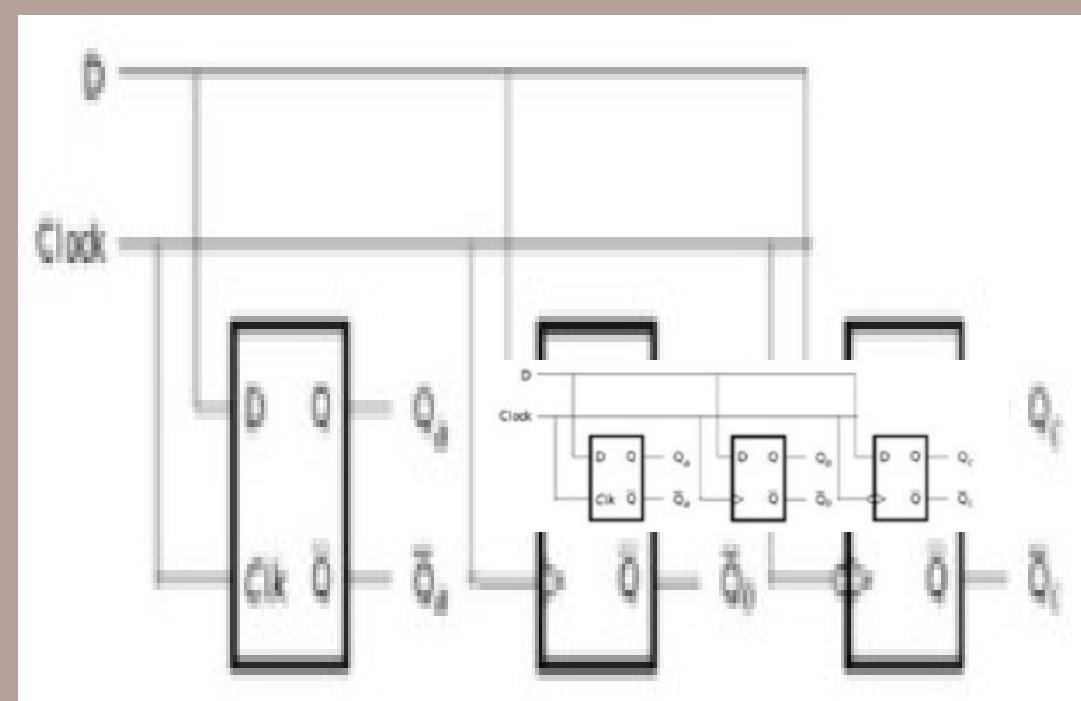
Rajah 1.



Rajah 3

EN	D	Q	Q ₊₁	STATE
1	0	0	0	RESET
1	0	1	0	
1	1	0	1	SET
1	1	1	1	
0	0	0	0	NC
0	0	1	1	
0	1	0	0	NC
0	1	1	0	

Rajah 2



Rajah 4

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Research Objective

To study the operation of D FLIP-FLOPS and to understand how reset and preset inputs can be added to any flip flop. Generate the next state equations and state tables for all types of FLIP-FLOPS.

Design of a D-Latch Flip-Flop

A D Flip Flop (also known as a D Latch or a 'data' or 'delay' flip-flop) is a type of [flip flop](#) that tracks the input, making transitions with match those of the input D. The D stands for 'data'; this flip-flop stores the value that is on the data line. It can be thought of as a basic memory cell.

In an active high [SR Flip Flop](#) is when S (Set) and R (Reset) both are 0, there will be no change in the output of the latch, and when both S and R are 1 the output of the latch is totally unpredictable. In an [active low SR Flip Flop](#) when S and R both are 1, there will be no change in the output of the latch, and when both S and R are 0 the output of the latch is totally unpredictable.

So if both inputs of the flip-flop are the same there will either be a *No Change* or *Invalid* output condition. If we avoid these conditions of inputs, there will be either SET or RESET conditions.

There are many applications, where only SET and RESET conditions of the latch are required. In these applications, we can use inputs (S and R) which are always the complement of each other.

This can be designed by a single input (S) to the latch and the R input achieved by inverting this S. This single input is called **data input** and it is labeled with D.

This is why this type of single input Flip flop is known as a D-Flip Flop or D Latch. The basic logical representation (i.e. circuit diagram) of a D-flip flop is shown on Rajah 1.

REFERENCES

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- [2] <https://www.digitalelectronicsdeeds.com/>
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