Digital Design Learning of SET-RESET FLIP FLOP with Deeds

Wan Mohd Hafiy Ikhwan Bin Azman, wanhafiy2030@gmail.com

Faculty of Communication, Visual Art and Computing
University Selangor

RESEARCH OBJECTIVE

This lab introduces the concept of sequential logic circuits and their basic working mechanisms. Students are expected to understand basic sequential circuits and the ways to measure delay time and set-up time of sequential logic circuits

HOW SR FLIP FLOP WORK

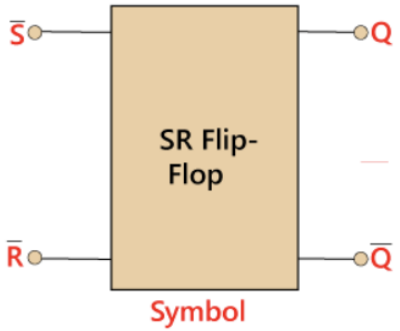
The SR flip flop stands for "Set-Reset" flip flop. The reset input is used to get back the flip flop to its original state from the current state with an output 'Q' like the symbol has shown(SR.1). This output depends on the set and resets conditions, which is either at the logic level "0" or "1".

The Set State

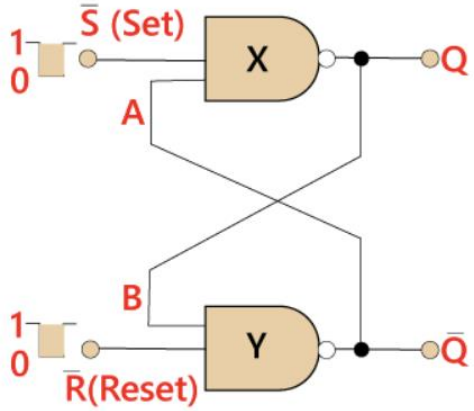
In the diagram SR.2, when the input R is set to false or 0 and the input S is set to true or 1, the NAND gate Y has an input 0, which will produce the output Q' 1. The value of Q' is faded to the NAND gate 'X' as input 'A', and now both the inputs of the NAND gate 'X' are 1(S=A=1), which will produce the output 'Q' 0.
Now, if the input R is changed to 1 with 'S' remaining 1, the inputs of NAND gate 'Y' is R=1 and B=0. Here, one of the inputs is also 0, so the output of Q' is 1. So, the flip flop circuit is set or latched with Q=0 and Q'=1.

Reset State

The output Q' is 0, and output Q is 1 in the second stable state. It is given by R =1 and S = 0. One of the inputs of NAND gate 'X' is 0, and its output Q is 1. Output Q is faded to NAND gate Y as input B. So, both the inputs to NAND gate *Y* are set to 1, therefore, Q' = 0.
Now, if the input S is changed to 0 with 'R' remaining 1, the output Q' will be 0 and there is no change in state. So, the reset state of the flip flop circuit has been latched, and the set/reset actions are defined in the following truth table in SR.3



SR.1



SR.2

State	S	R	Q	Q'	Description
Set	1	0	0	1	Set Q'>>1
	1	1	0	1	No change
Reset	0	1	1	0	Reset Q'>>0
	1	1	1	0	No change
Invalid	0	0	1	1	Invalid Condition

SR.3

REFERENCES

[1] Manual Pengguna, (2022). Aplikasi Pendidikan dan Reka Bentuk Elektronik Digital (S. Widyarto, Ed. & Trans.; 1st ed.). International Community Forum (ICF).
[2] https://www.digitalelectronicsdeeds.com/
[3] https://www.javatpoint.com/sr-flip-flop-in-digital-electronics

ICF

INTERNATIONAL COMMUNITY FORUM (ICF)

Deeds-DcS Digital Circuit Simulator