

# Decoder (2-4)

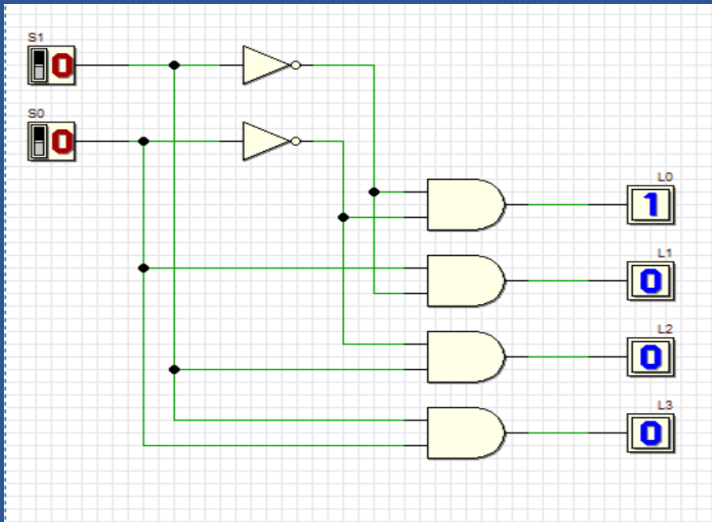


Figure 1

Inputs		Outputs			
s0	s1	L0	L1	L2	L3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

Figure 2

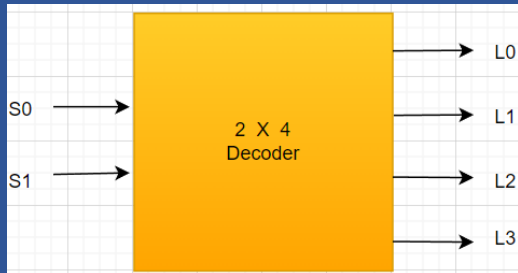


Figure 3

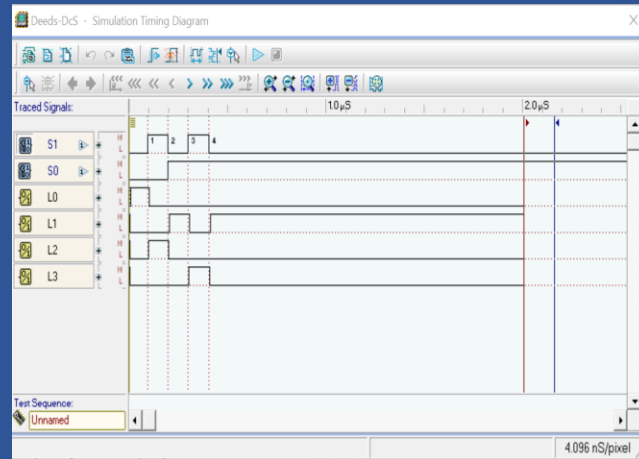


Figure 4

## Re-thinking a synchronous counter as Finite State Machine.

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### Objective

- To use decoders to implement logic functions.
- To use multiplexers to implement logic functions.
- To use BCD-to-7 segment decoder.

### DESIGN OF A GENERATOR THAT CAN BE PROGRAMMED PERIODICAL SEQUENCE.

The binary inputs s1 and s0 determine which output line from L0 to L3 is “HIGH” at logic level “1” while the remaining outputs are held “LOW” at logic “0” so only one output can be active (HIGH) at any one time. Therefore, whichever output line is “HIGH” identifies the binary code present at the input, in other words it “decodes” the binary input. Some binary decoders have an additional input pin labelled “Enable” that controls the outputs from the device. This extra input allows the decoders outputs to be turned “ON” or “OFF” as required. Output is only generated when the Enable input has value 1; otherwise, all outputs are 0. Only a small change in the implementation is required: the Enable input is fed into the AND gates which produce the outputs. If Enable is 0, all AND gates are supplied with one of the inputs as 0 and hence no output is produced. When Enable is 1, the AND gates get one of the inputs as 1, and now the output depends upon the remaining inputs. Hence the output of the decoder is dependent on whether the Enable is high or low. Finally, Figure 1 is containing schematic diagram, Figure 2 Contains truth table, Figure 3 containing Line decoder and Figure 4 is containing timing diagram.

### References

- [1] Manual Pengguna, (2022). Aplikasi Pendidikan dan Reka Bentuk Elektronik Digital (S. Widyarto, Ed. & Trans.; 1st ed.). International Community Forum (ICF).
- [2] <https://www.digitalelectronicsdeeds.com/>
- [3] <https://www.allaboutcircuits.com/textbook/digital/chpt-9/decoder/>