

Learn Digital Design of Microcomputer Systems with Deeds

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RESEARCH OBJECTIVE

The purpose of this lab is to delay the change of state of its output signal (Q) until the next rising edge of a clock timing input signal occurs in

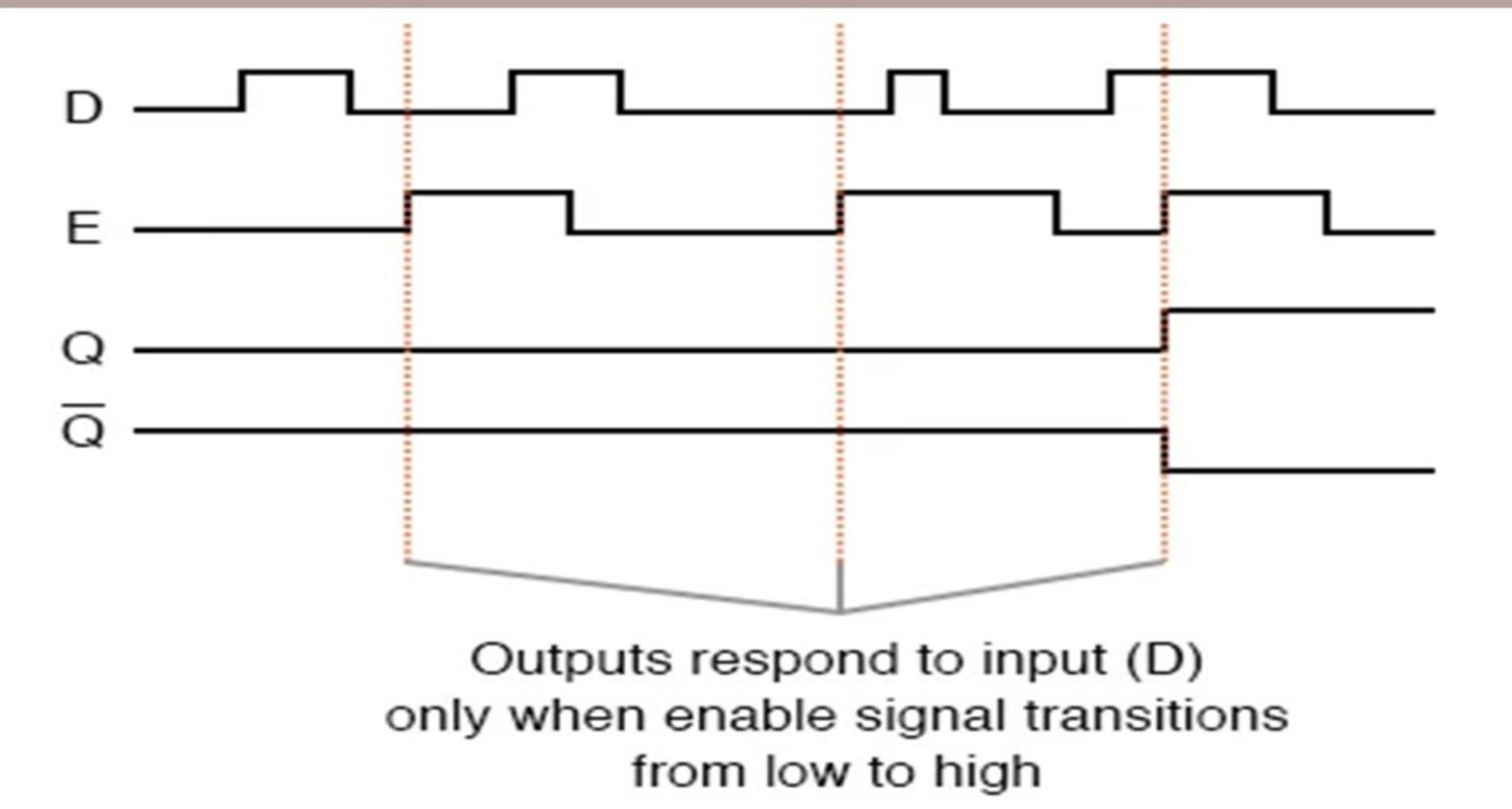
Figure 1

ANALYSIS OF A D-Latch flip-flop

D Flip-flops are used as a part of memory storage elements and data processors as well. D flip-flop can be built using NAND gate or with NOR gate. Due to its versatility they are available as IC packages. The major applications of D flip-flop are to introduce delay in timing circuit, as a buffer, sampling data at specific intervals. D flip-flop is simpler in terms of wiring connection compared to JK flip-flop. Here we are using NAND gates for demonstrating the D flip flop. Whenever the clock signal is LOW, the input is never going to affect the output state. The clock has to be high for the inputs to get active. Thus, D flip-flop is a controlled Bi-stable latch where the clock signal is the control signal. Again, this gets divided into positive edge triggered D flip flop and negative edge triggered D flip-flop. The D(Data) is the input state for the D flip-flop. The Q and Q' represents the output states of the flip-flop. According to the truth table, based on the inputs the output changes its state. But, the important thing to consider is all these can occur only in the presence of the clock signal. This, works exactly like SR flip-flop for the complimentary inputs alone.

REFERENCES

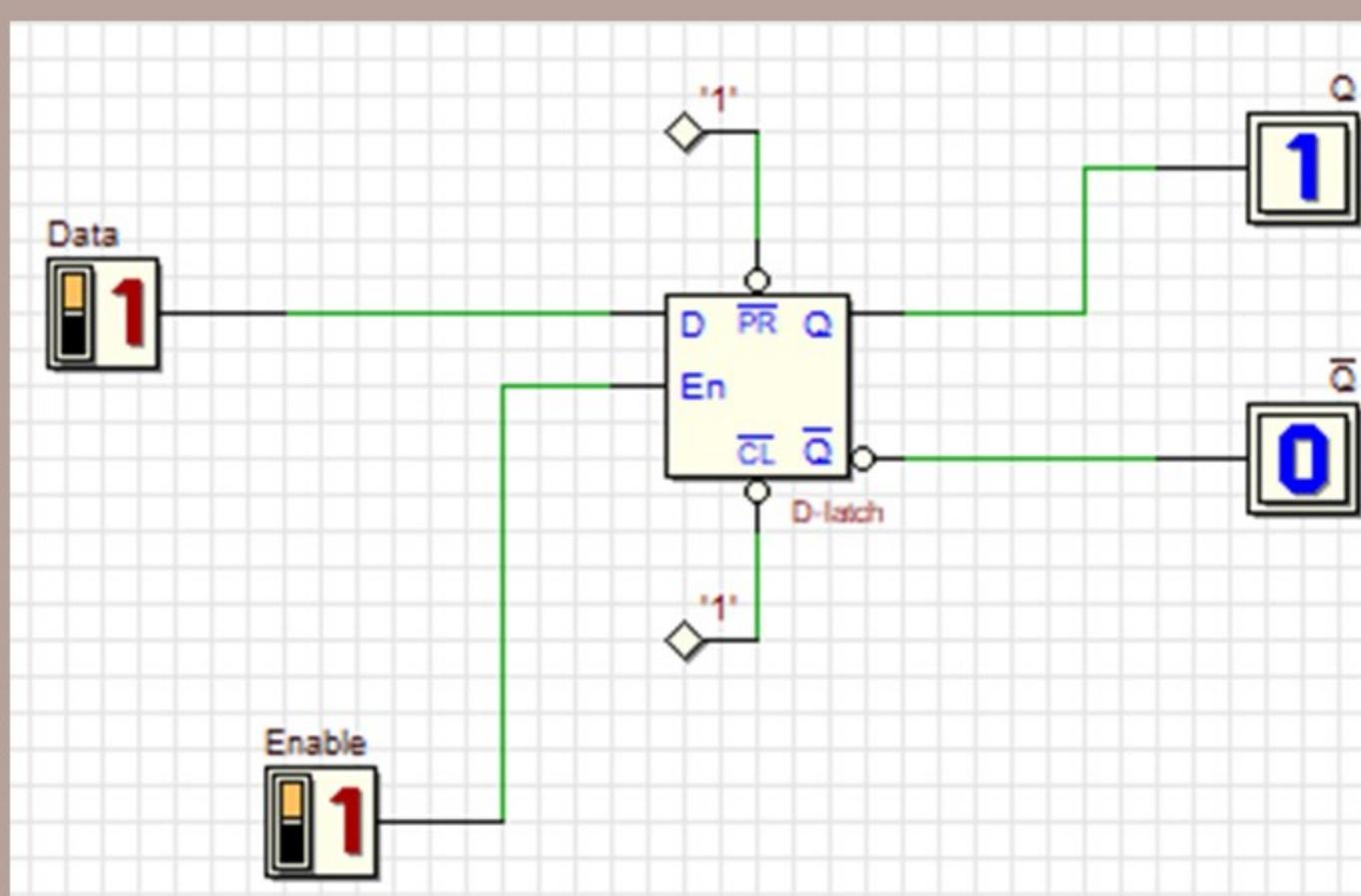
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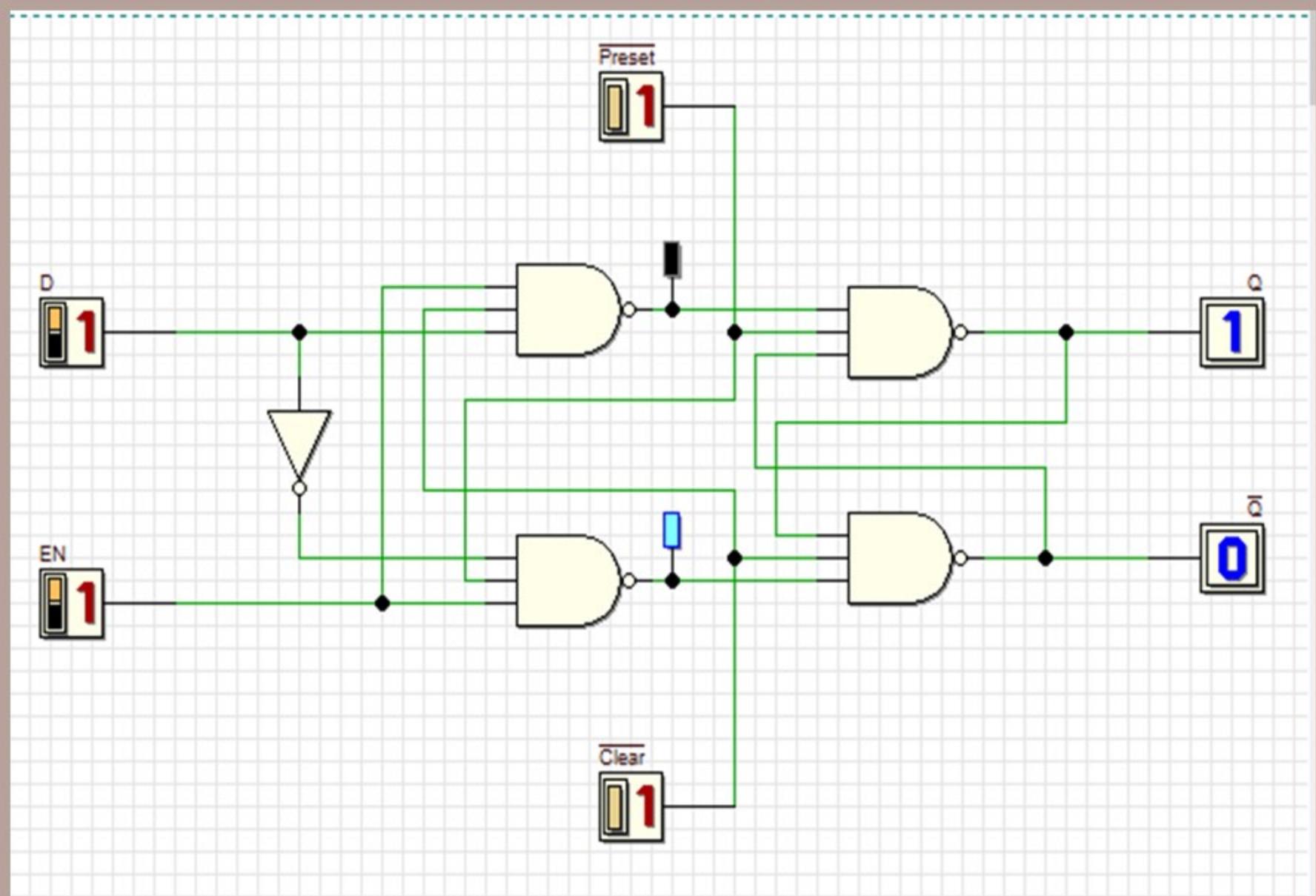
Timing Diagram

Clk	D	Q	\bar{Q}	Description
$\downarrow \gg 0$	X	Q	\bar{Q}	Memory no change
$\uparrow \gg 1$	0	0	1	Reset Q $\gg 0$
$\uparrow \gg 1$	1	1	0	Set Q $\gg 1$

Truth Table of D Flip-Flop



D-Latch flip-flop component



Analysis of a D-Latch flip-flop



INTERNATIONAL COMMUNITY FORUM (ICF)

