Learn to Design Digital Electronics with Deeds

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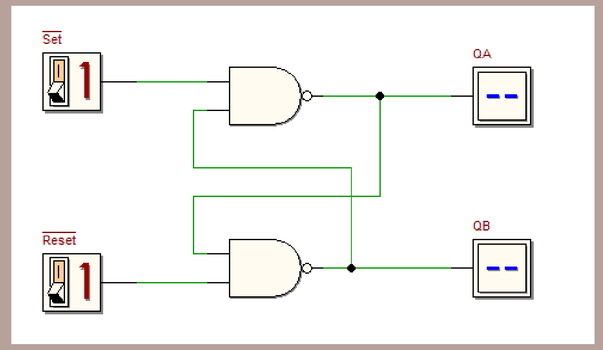
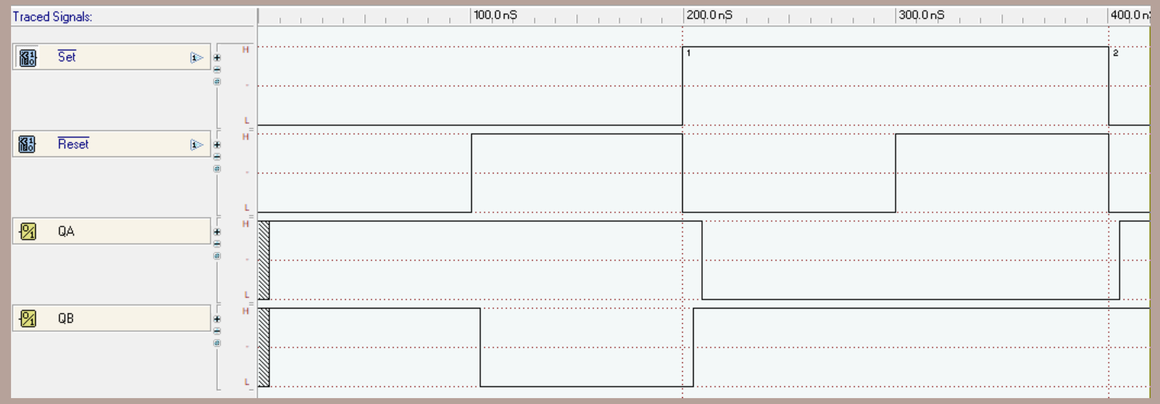


Schematic Diagram



Timing Diagram

S	R	QA	QB
0	0	1	1
0	1	1	0
1	0	0	1
1	1	0	1
		1	0

Truth Table

RESEARCH OBJECTIVE

The purpose of this lab is to analyse a **Set-Reset flip-flop** schematic in the **d-DcS**.

To verify the behavior of the flip flop using the **timing simulation**,

present all the possible combinations of inputs, using a proper time scale (a suitable **test sequence** in the **Timing Diagram window**) and to explain why the circuit shows a stable auto-oscillation, and why it can not happen in the 'real world'

Analysis of a Set-Reset flip-flop

!Set and **!Reset** are kept high most of the time. When input !Set is made low momentarily 1 to 0, the output QA becomes 1. The Set-Reset flip-flop is now storing a 1 and !Set can be returned to its normal high state. When input !Reset is made low momentarily 1 to 0, the output QB becomes 1. The Set-Reset flip-flop is now storing a 1 and !Reset can be returned to its normal high state.

The NAND gate Set-Reset flip-flop is set or reset with low logic, that is its an active low Set-Reset flip-flop

It has a forbidden state that is when both !Set and !Reset are simultaneously 0. This would result in an illegal state in which both QA and QB are one. The circuit will show a stable auto-oscillation. It is Invalid. It cannot happen the real world.

REFERENCES

[1] Manual Pengguna, (2022). Aplikasi Pendidikan dan Reka Bentuk Elektronik Digital (S. Widyarto, Ed. & Trans.; 1st ed.). International Community Forum (ICF).

[2] https://www.digitalelectronicsdeeds.com/

ICF

INTERNATIONAL COMMUNITY FORUM (ICF)

Deeds-DcS
Digital Circuit Simulator

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