

Learn Digital Design of Microcomputer Systems with Deeds

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Research objective

The purpose of this lab is to design a programmable multiphase square wave generator. It generates three cyclic signals, UA, UB and UC, like the time cycle of Figure

Classification of Sequential Logic

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As standard logic gates are the building blocks of combinational circuits, bistable latches and flip-flops are the basic building blocks of sequential logic circuits. Sequential logic circuits can be constructed to produce either simple edge-triggered flip-flops or more complex sequential circuits such as storage registers, shift registers, memory devices or counters. Either way sequential logic circuits can be divided into the following three main categories:

- 1. Event Driven – asynchronous circuits that change state immediately when enabled.
- 2. Clock Driven – synchronous circuits that are synchronised to a specific clock signal.
- 3. Pulse Driven – which is a combination of the two that responds to triggering pulses.

SR Flip-Flop

The **SR flip-flop**, also known as a *SR Latch*, can be considered as one of the most basic sequential logic circuit possible. This simple flip-flop is basically a one-bit memory bistable device that has two inputs, one which will “SET” the device (meaning the output = “1”), and is labelled S and one which will “RESET” the device (meaning the output = “0”), labelled R. Then the SR description stands for “Set-Reset”. The reset input resets the flip-flop back to its original state with an output Q that will be either at a logic level “1” or logic “0” depending upon this set/reset condition. A basic NAND gate SR flip-flop circuit provides feedback from both of its outputs back to its opposing inputs and is commonly used in memory circuits to store a single data bit. Then the SR flip-flop actually has three inputs, Set, Reset and its current output Q relating to it’s current state or history. The term “Flip-flop” relates to the actual operation of the device, as it can be “flipped” into one logic Set state or “flopped” back into the opposing logic Reset state.

REFERENCES

- [1] <https://www.digitalelectronicsdeeds.com/>
- [2] https://www.electronics-tutorials.ws/sequential/seq_1.html
- [3] Manual Pengguna, (2022). Aplikasi Pendidikan dan Reka Bentuk Elektronik Digital (S Widyarto, Ed. & Trans.; 1st ed.). International Community Forum (ICF).

Set-Reset flip-flop

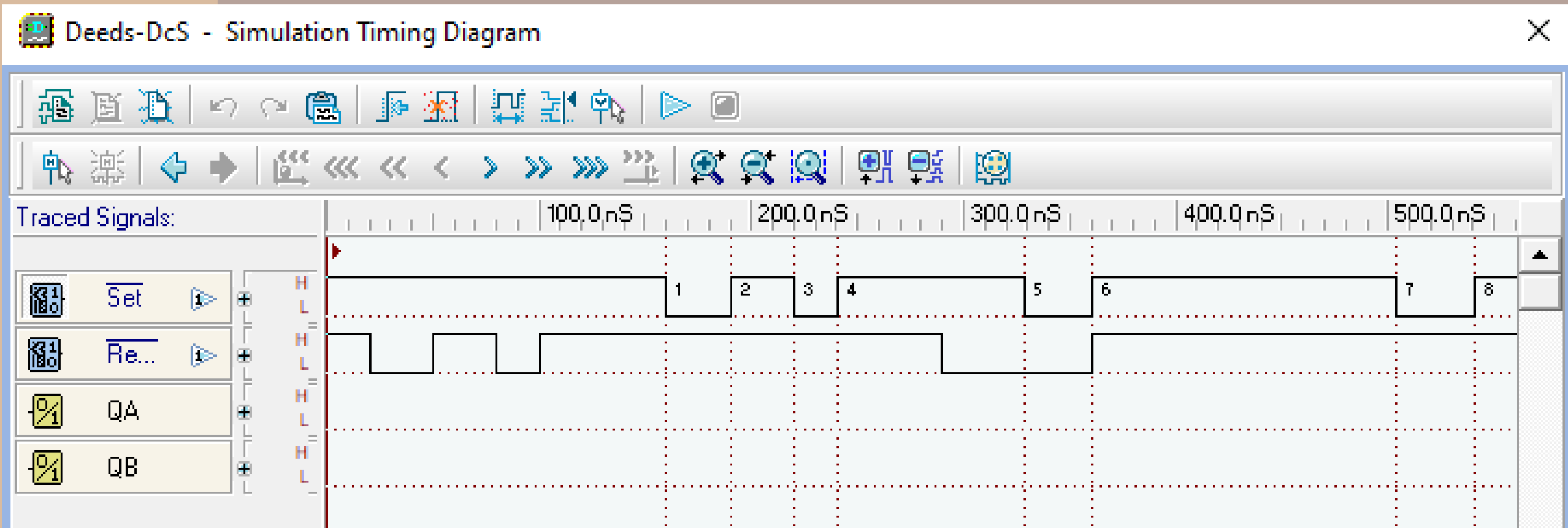


Diagram 1.

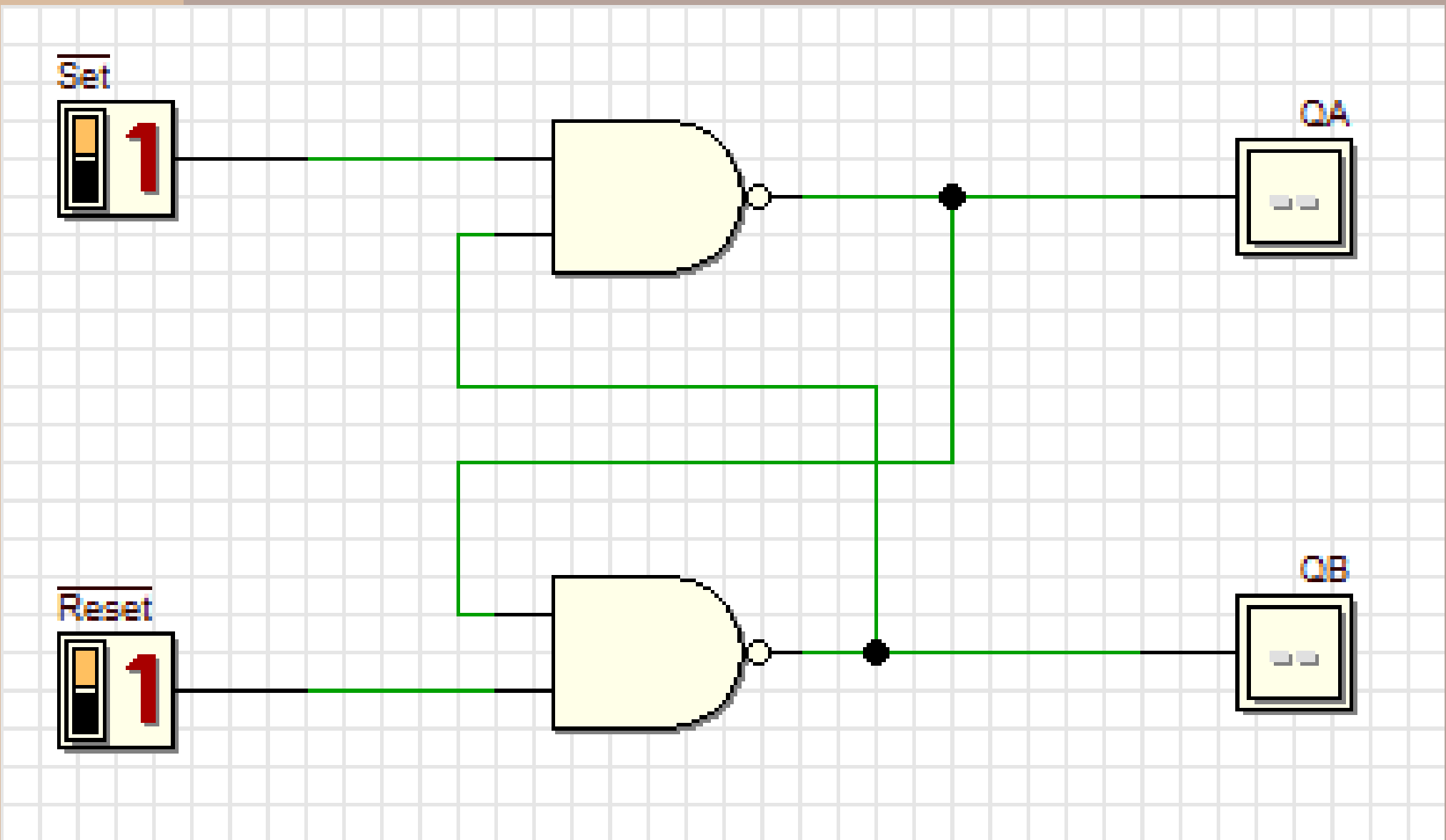


Diagram 2

Set	Reset	QA	QB
0	0	1	1
0	1	1	0
1	0	0	1
1	1	1	0

Diagram 3.



INTERNATIONAL COMMUNITY FORUM (ICF)

