Learn The Analysis Of A JK-Flip-Flop With Deeds

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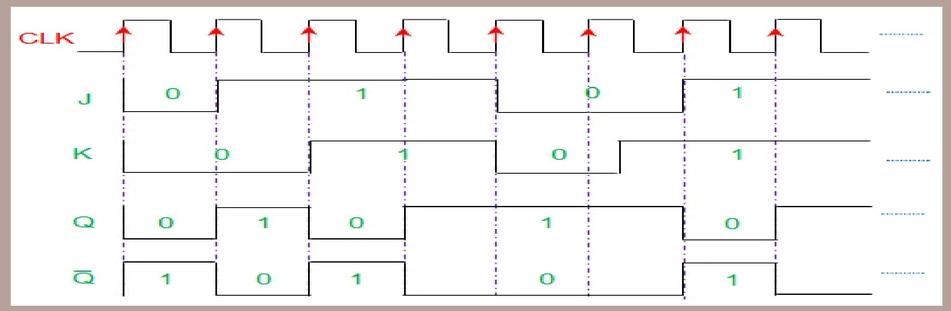

Diagram 1.

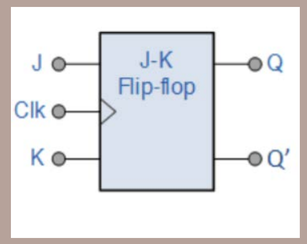

Diagram 2.

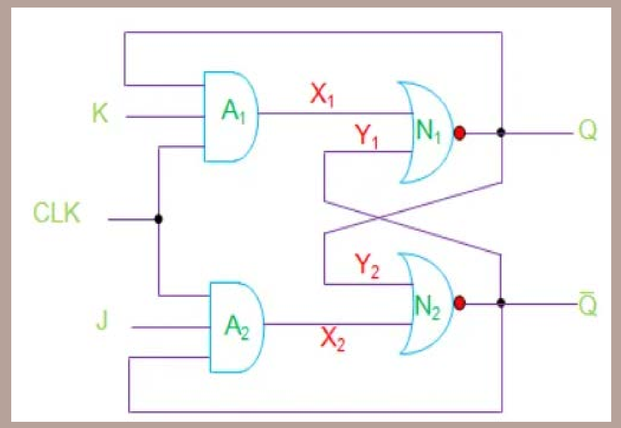

Diagram 3.

Truth Table

Trigger	Inputs		Output				Inference
			Present State		Next State		
CLK	J	K	Q	Q̄	Q	Q̄	
↑	x	x	-		-		Latched
↑	0	0	0	1	0	1	No Change
↑			1	0	1	0	
↑	0	1	0	1	0	1	Reset
↑			1	0	0	1	
↑	1	0	0	1	1	0	Set
↑			1	0	1	0	
↑	1	1	0	1	1	0	Toggles
↑			1	0	0	1	

Diagram 4.

RESEARCH OBJECTIVE

This lab introduces the concept of sequential logic circuits and their basic working mechanisms. Students are expected to understand to design a sequential logic circuit using JK-Flip-Flop and to implement the designed circuit.

MECHANISME OF A JK-FLIP-FLOP

In order to have an insight over the working of JK flip-flop, it has to be realized in terms of basic gates similar to that in Diagram 2 which expresses a positive-edge triggered **JK flip-flop** using AND gates and NOR gates. Here, it can be observed that the output Q and the clock pulse are logically anded using the AND gate 1, A1, whereas the output $\bar{Q}$ is anded using the clock pulse and the input J. (using AND gate 2, A2). Further the output of A_1 is fed as one of the inputs (X_1) to the NOR gate 1, N_1 whose other input (Y_1) is connected to output $\bar{Q}$. Similarly NOR gate 2, N2 has its two inputs (X2 and Y2) as the output of A_2 and output Q (respectively). Initially let J = K = 0, Q = 0 and $\bar{Q}$ = 1. Now consider the appearance of positive-edge of the first clock pulse at the CLK pin of the flip-flop. This results in X_1 = 0 and X_2 = 0. Then the output of N_1 will become 0 as X_1 = 0 and $\bar{Q}$ = 1; while the output of N_2 will become 1 as X_2 = 0 and Q = 0. Thus one gets Q = 0 and $\bar{Q}$ = 1. However if one considers the initial states to be J = K = 0, Q = 1 and $\bar{Q}$ = 0, then $X_1 = X_2 = 0$ which results in Q = 1 and $\bar{Q}$ = 0. This indicates that the state of flip-flop outputs Q and $\bar{Q}$ remains unchanged for the case of J = K = 0.

Now assume that J = 0, K = 1, Q = 0 and $\bar{Q}$ = 1. Analyzing on the same grounds, one gets $X_1 = X_2 = 0$ which further results in Q = 0 (and hence $\bar{Q}$ = 1). For the same case if Q and $\bar{Q}$ were 1 and 0, respectively, then X_1 = 1 and X_2 = 0 which would result in Q = 0 (and hence $\bar{Q}$ = 1).

This implies that if J = 0 and K = 1, then the flip-flop resets (Q = 0 and $\bar{Q}$ = 1).
Next if J = 1, K = 0, Q = 1 and $\bar{Q}$ = 0, then $X_1 = X_2 = 0$ which results in Q = 1 (and thus $\bar{Q}$ = 0). For the same case if Q = 0 and $\bar{Q}$ = 1, then X_1 = 0, X_2 = 1 which leads to $\bar{Q}$ = 0 and hence Q is forced to value 1. This means that for the case of J = 1 and K = 0, flip-flop output will always be set i.e. Q = 1 and $\bar{Q}$ = 0.

Similarly for J = 1, K = 1, Q = 1 and $\bar{Q}$ = 0 one gets X_1 = 1, X_2 = 0 and Q = 0 (and hence $\bar{Q}$ = 1); and if Q changes to 0 and $\bar{Q}$ to 1, then X_1 = 0, X_2 = 1 which forces $\bar{Q}$ to 0 and hence Q to 1. This indicates that for J = K = 1, flip-flop outputs toggle meaning which Q changes from 0 to 1 or from 1 to 0, and these changes are reflected at the output pin $\bar{Q}$ accordingly.

REFERENCES

[1] Manual Pengguna, (2022). Aplikasi Pendidikan dan Reka Bentuk Elektronik Digital (S. Widyarto, Ed. & Trans.; 1st ed.). International Community Forum (ICF).

[2] https://www.digitalelectronicsdeeds.com/

[3] https://www.electrical4u.com/jk-flip-flop/

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