

Digital Design Learning of SR Latch Flip Flop with Deeds

Nur Allysa Adeera, 3212013381@istudent.unisel.edu.my

Faculty of Communication, Visual Art and Computing
Universiti Selangor

RESEARCH OBJECTIVE

- To design various latch and flip-flop circuits
- To test various latch and design circuits
- To measure the non-ideal properties of your circuits and compare the performance of your flip-flop(s) with that of a pre-packaged flip-flop.

MOST SIMPLE TYPE OF FLIP FLOP

A bistable multivibrator has two stable states, as indicated by the prefix bi in its name. Typically, one state is referred to as set and the other as reset. The simplest bistable device, therefore, is known as a set-reset, or S-R, latch. To create an S-R latch, we can wire two NOR gates in such a way that the output of one feeds back to the input of another, and vice versa, like Image 1.

The Q and not-Q outputs are supposed to be in opposite states. I say “supposed to” because making both the S and R inputs equal to 1 results in both Q and not-Q being 0. For this reason, having both S and R equal to 1 is called an invalid or illegal state for the S-R multivibrator.

Otherwise, making S=1 and R=0 “sets” the multivibrator so that Q=1 and not-Q=0. Conversely, making R=1 and S=0 “resets” the multivibrator in the opposite state. When S and R are both equal to 0, the multivibrator’s outputs “latch” in their prior states.

Note how the same multivibrator function can be implemented in ladder logic, with the same results (Image 2)

REFERENCES

- [1] Manual Pengguna, (2022). Aplikasi Pendidikan dan Reka Bentuk Elektronik Digital (S. Widjarto, Ed. & Trans.; 1st ed.). International Community Forum (ICF).
- [2] <https://www.digitalelectronicsdeeds.com/>



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