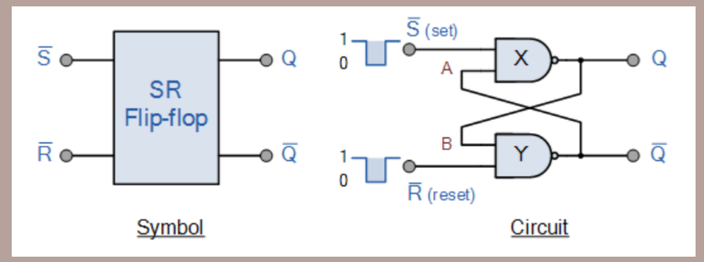
Learn the analysis of a Set-Reset flip-flop with Deeds

Nur Insyirah Syamila, insyirahsyamila3800@gmail.com

Faculty of Communication, Visual Art and Computing

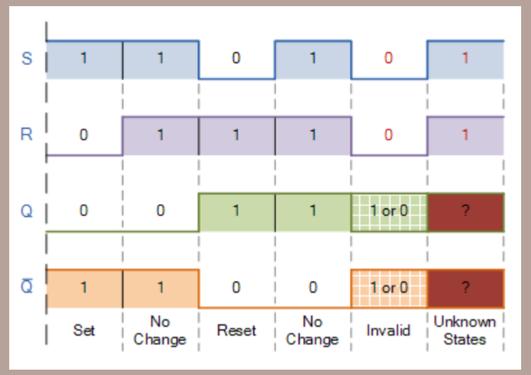
Universiti Selangor



Rajah 1.

State	S	R	Q	$\overline{Q}$	Description
Set	1	0	0	1	Set $\overline{Q}$ » 1
	1	1	0	1	no change
Reset	0	1	1	0	Reset $\overline{Q}$ » 0
	1	1	1	0	no change
Invalid	0	0	1	1	Invalid Condition

Rajah 2



Rajah 3.

RESEARCH OBJECTIVE

This lab introduces the concept of sequential logic circuits and their basic working mechanisms. Students are expected to understand basic sequential circuits and the ways to measure delay time and set-up time of sequential logic circuits.

MECHANISMS OF A SR FLIP FLOP

The Set State

Consider the circuit shown. If the input R is at logic level "0" (R = 0) and input S is at logic level "1" (S = 1), the NAND gate *Y* has at least one of its inputs at logic "0" therefore, its output Q must be at a logic level "1" (NAND Gate principles). Output Q is also fed back to input "A" and so both inputs to NAND gate *X* are at logic level "1", and therefore its output Q must be at logic level "0".

Again NAND gate principals. If the reset input R changes state, and goes HIGH to logic "1" with S remaining HIGH also at logic level "1", NAND gate *Y* inputs are now R = "1" and B = "0". Since one of its inputs is still at logic level "0" the output at Q still remains HIGH at logic level "1" and there is no change of state. Therefore, the flip-flop circuit is said to be "Latched" or "Set" with Q = "1" and Q = "0".

Reset State

In this second stable state, Q is at logic level "0", (not Q = "0") its inverse output at Q is at logic level "1", (Q = "1"), and is given by R = "1" and S = "0".

As gate *X* has one of its inputs at logic "0" its output Q must equal logic level "1" (again NAND gate principles). Output Q is fed back to input "B", so both inputs to NAND gate *Y* are at logic "1", therefore, Q = "0".

If the set input, S now changes state to logic "1" with input R remaining at logic "1", output Q still remains LOW at logic level "0" and there is no change of state. Therefore, the flip-flop circuits "Reset" state has also been latched and we can define this "set/reset" action in the following truth table.

REFERENCES

[1] Manual Pengguna, (2022). Aplikasi Pendidikan dan Reka Bentuk Elektronik Digital (S. Widyarto, Ed. & Trans.; 1st ed.). International Community Forum (ICF).

[2] https://www.digitalelectronicsdeeds.com/

{3} https://www.electronics-tutorials.ws/sequential/seq_1.html

ICF

INTERNATIONAL COMMUNITY FORUM (ICF)

Deeds-DcS Digital Circuit Simulator

unisel UNIVERSITI SELANGOR